

⇒⇒ Digitimes

"All the news that's fit to encapsulate"

Vol. III, No. 3

Across the Desk

CUSTOMERS QUEUE FOR Q-SERIES



From the Engineer's Notebook

HIGH-COUNT HYBRID and VALLEY DETECTOR



Ad of the Month

FIVE \$ FLIP-FLOP

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Big Breakthrough

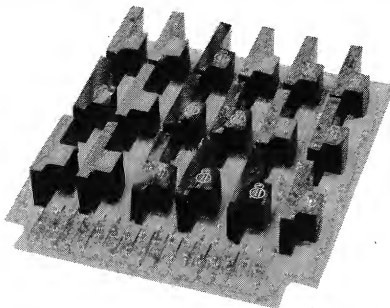
Beats Budget Blues

We have been pacing up and down wringing our hands worrying about the startling reduction in price recently announced by one of the integrated circuit manufacturers. The end is here! Doom and misery!

In the midst of our pacing there came a tapping on the door. We opened it to let the raven in, but found instead one of our line supers. He strode in through the gloom and placed a small encapsulated circuit on our desk. "What's your estimate of the labor time?" he sez.

As an old estimator, we muttered the proper incantations and came up with "x" minutes. "Divide 'x' by 5," said Tom. (We won't say swiftly!) The gloom vanished, and we forgot the raven completely.

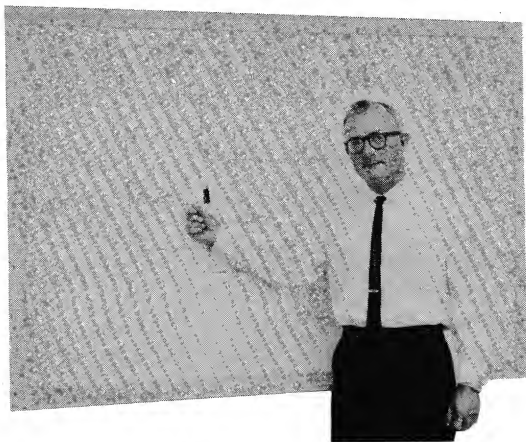
Several days later we put down our smoking slide rules and decided that we now have a low cost* line (if you call three circuits a line) of digital NAND/NOR circuits that will satisfy 99% of your digital requirements with only three different circuits (guess it is a line if it will do all that).



Think about it — you have created this vast system with thousands of flip-flops, hundreds of shift registers, miny miny gates, etc., and there you stand surveying your empire with a complete set of spares in your coat pocket; or was that the coat you sent to the cleaners this morning? No matter; you, as a clear thinking planner ahead, have another complete set of spares in your desk drawer. Additional investment? Ten bucks including the set at the cleaners. Begin to see the advantages? No more loading charts, no more thumbing through hundreds of pages of closely

*Lower than the lowest integrated with no derating of specs.

written do's and don't's, no more "If I do this, will it do that?" All you have to do is learn a **very few** simple rules, the significance of a **very few** pin numbers, and you are in business.



Get to your file cabinet and haul out all of those applications that were "too expensive to be practical" and check them out again using the Q Series. We think you will be in for a very pleasant surprise. You had better hurry. As of this writing the line has not yet been announced, and we have two orders in the house.

Integrated circuits? What are they?

— J. E. McCloskey

ECCo General Sales Manager

A PEEK AT VALLEY DETECTION

Here is a tricky circuit, designed to satisfy a recent application request, that monitors an analog input and tallies the number of times it dips below -1 v, -2 v, etc. A desired feature was that no count be registered as being below, say -1 v, if the input continued to dip below any relatively lower threshold, -2 v, for example.

The answer arrived at for a five channel device uses five T-174 Voltage Comparators, two T-136 Inverters, four T-162 RS Flip-Flops and two T-448 Dual Pulse "AND" Gates, in addition to five N-102 Decade Counters. More can be used if more than ten valleys are expected in a given observation period.

To visualize how the circuit works, consider the case where the input falls below -3 v but does not fall below -4 v. The T-174's are biased to the desired sensing levels (-1 v, -2 v, etc.). These are the initial conditions:

- A circuit has reset all decade counters to zero and set the flip-flops so that their outputs are in the "1" state (-3 v).
- Outputs of the T-174's rest at -3 v because the input voltage is more positive than the various sensing levels.

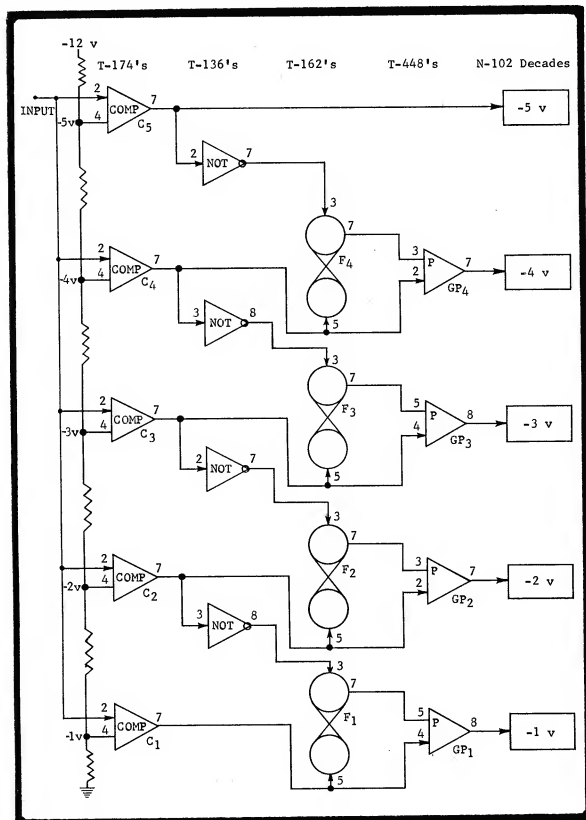
As the input moves in a negative direction, the outputs of comparators C_1 , C_2 , and C_3 shift to -11 v as each reference level, respectively, is encountered. The "false" output of C_2 , inverted by half of a T-136, resets flip-flop F_1 , which then outputs GP_1 . Similarly, as the input falls below each reference level, the preceding counter is disabled.

No count is registered during this phase because no yet occurred. A "valley" is sensed when the input begins moving in the positive direction. As it returns reference level reached, the related comparator produces an output, which is gated to the corresponding counter one count. As the input continues to rise toward 0 v outputs of higher level comparators (C_2 and C_1 , for example) and their related flip-flops, restoring initial conditions. Because the related gates have been disabled during the negative excursion, no counts are made by succeeding dips.

With the reference levels chosen here, this circuit tallies the number of valleys between each of the following ranges:

- -1 v to -2 v
- -2 v to -3 v
- -3 v to -4 v
- -4 v to -5 v
- less than -5 v

Puzzler of the month: How would you change the circuit to be a positive peak counter?



MULTI-BIT COMPARATOR GOES ANALOG

Requests for multi-bit comparator circuits have been heavy recently. One of them, a kind of "hybrid" approach, is quite interesting.

The problem was to design a circuit capable of storing the highest in a series of numbers fed to it. While this particular application uses a single decade counter and shift register, the idea could be extended, of course, to handle larger numbers. Here is how the circuit operates.

Within a specified period, a train of pulses is counted by a 1-2-4-8 decade; at the end of the count period, the number is compared with a previously stored number. If the number stored exceeds the count in the counter, the counter is simply reset preparatory to another count period. If, on the other hand, the number stored (in a shift register) does **not** exceed the count in the counter, then this higher count is transferred to the shift register before the counter is reset preparatory to another count cycle.

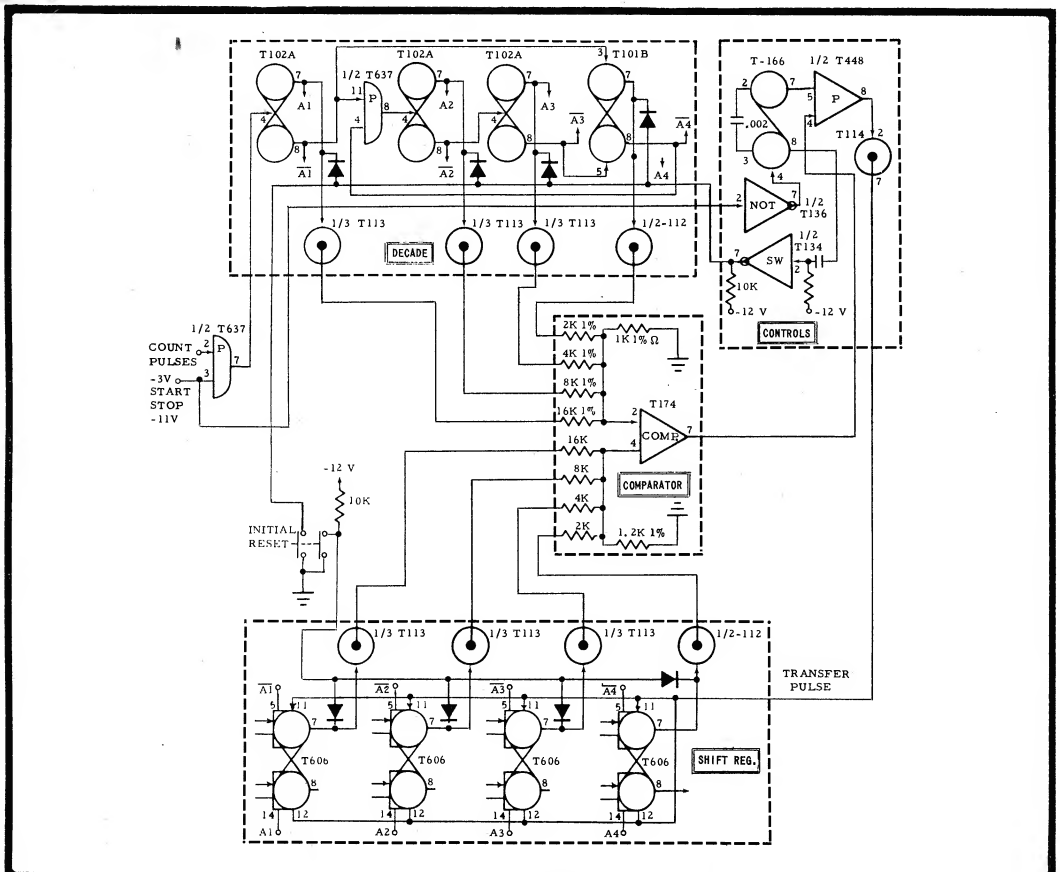
As shown, the circuit consists of a decade counter, a shift register, a comparator, and control circuits. Input pulses and the "start/stop" control signal that determines each count period are gated to the counter through a "pulse and" gate (half of a T637).

Because extreme accuracy was not significant in this application, a money-saving method of comparison was adopted. Outputs of the decade and shift register are applied to resistive summing networks and the resulting analog voltages are coupled to a T-174 voltage comparator.

If the count in the decade exceeds that in the shift register, a pulse is sent to a gate (half of a T-448) and emitter follower (a T-114) which triggers a parallel shift of the "count" into the shift register. **When** the "shift" decision is made is controlled by a one shot (a T-166) with a duration sufficient for the transfer to be completed. The one-shot's return to the stable state triggers collector reset of the counter (through a T-134) to begin the next cycle.

The one-shot multivibrator derives its input, through an inverter (half of a T-136), from the negative-going "start/stop" level. Note that if the "count" period were accurately known, the delay of the one-shot could have been adjusted to equal it, and thus, have been triggered instead by the positive-going "start" pulse. This would have eliminated need for the T-136.

The shift register can be wired for serial or parallel output, and, as a final touch, R-341 or 342 Minisig Indicators can be added for monitoring the goings on.



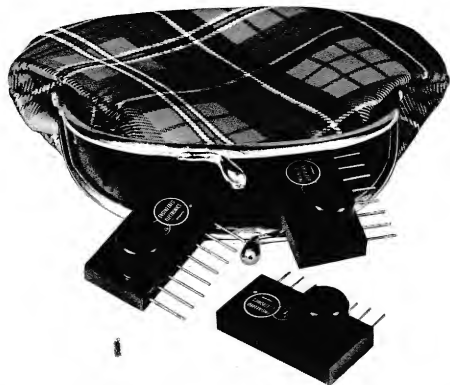
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Ad-of-the-Month

3Q = 99%

The news is out... far and wide. EECO's new Q-Series is set to rock the flip-flop industry with rock-bottom prices. Imagine — a flip-flop for less than a FIVER. Fantastic! Capable of serving 99 per cent of logic needs through wiring combinations of just three encapsulated building blocks, the unique series goes further by sparing you stock and spare expense.

For more details look for this ad in the July issues of **ELECTRONIC DESIGN** and **ELECTRICAL DESIGN NEWS**.

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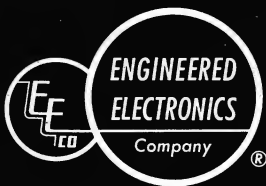
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